SEMICONDUCTOR MEMORY DEVICE AND METHOD OF OPERATING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to: (1) U.S. Provisional Application Serial No.

5 60/470,384, entitled "Method of Operating Semiconductor Memory Device", filed May 13,

2003; and (2) U.S. Provisional Application Serial No. 60/470,318, entitled "Dual Port One

Transistor DRAM Memory Cell and Extension to Multi-Port Memory Cell", filed May 13,

2003 (hereinafter collectively "the Provisional Applications"). The contents of the

Provisional Applications are incorporated by reference herein in their entirety.

10 ## BACKGROUND

This invention relates to a semiconductor dynamic random access memory

("DRAM") cell, array and/or device and method of controlling and/or operating a

semiconductor memory cell array and/or device; and more particularly, in one aspect, to a

semiconductor dynamic random access memory ("DRAM") cell, array and/or device

15 wherein the memory cell includes an electrically floating body in which an electrical charge

is stored.

There are many different types and/or forms of DRAM cells, including, for example, a

semiconductor memory cell consisting of an access transistor and a capacitor, which stores

an electric charge representing a bi-stable memory state. The access transistor serves as

20 a switch for controlling the charging and discharging of the capacitor as well as reading and

writing of the logic states into the capacitor (i.e., charging or discharging the capacitor).

Although significant integration densities can be achieved with DRAM devices employing one transistor - one capacitor memory cells, such devices tend to be limited or restricted with respect to the size of the memory cell. In this regard, conventional techniques employ stacked and/or trench capacitor approaches, whereby the capacitor is

5   partially disposed above and/or below an access transistor.

In addition, DRAM devices employing one transistor - one capacitor memory cells tend to be fabricated using manufacturing processes that are different from and/or incompatible with manufacturing processes for logic devices (for example, microprocessors). As a result, integration of one transistor - one capacitor memory cells

10   into logic devices is often complicated and expensive.

Another type of dynamic random access memory cell is described and illustrated in non-provisional patent application entitled "Semiconductor Device", which was filed on June 10, 2003, and assigned Serial No. 10/450,238 (hereinafter "Semiconductor Memory Device Patent Application"). With reference to FIGURES 1A and 1B, the Semiconductor Memory

15   Device Patent Application discloses, among other things, semiconductor DRAM device 10 in which each memory cell 12 consists of transistor 14 having gate 16, body region 18, which is electrically floating, source region 20 and drain region 22. The body region 18 is disposed between and adjacent to source region 20 and drain region 22. Data is written into or read from a selected memory cell by applying suitable control signals to a selected

20   word line(s) 24, a selected source line(s) 26 and/or a selected bit line(s) 28. In response, charge carriers are accumulated in or emitted and/or ejected from electrically floating body region 18 wherein the data states are defined by the amount of carriers within electrically floating body region 18.

In particular, in one embodiment, the memory cell of the Semiconductor Memory Device Patent Application operates by accumulating in or emitting/ejecting majority carriers (electrons or holes) 30 from body region 18 of N-channel transistors. (See, FIGURES 2A and 2B). In this regard, accumulating majority carriers (in this example, "holes") 30 in body region 18 of memory cells 12 via, for example, impact ionization near source region 20 and/or drain region 22, is representative of a logic high or "1" data state. (See, FIGURE 2A). Emitting or ejecting majority carriers 30 from body region 18 via, for example, forward biasing the source/body junction and/or the drain/body junction, is representative of a logic low or "0". (See, FIGURE 2B).

Various techniques may be employed to read the data stored in (or write the data into) a memory device of the Semiconductor Memory Device Patent Application. For example, a current sense amplifier (not illustrated) may be employed to read the data stored in memory cells 12. In this regard, a current sense amplifier may compare the memory cell current to a reference current, for example, the current of a reference cell (not illustrated). From that comparison, it may be determined whether memory cell 12 contained a logic high (relatively more majority carriers 30 contained within body region 18) or logic low data state (relatively less majority carriers 28 contained within body region 18).

Notably, transistor 14 may be a symmetrical or non-symmetrical device. Where transistor 14 is symmetrical, the source and drain regions are essentially interchangeable. However, where transistor 14 is a non-symmetrical device, the source or drain regions of transistor 14 have different electrical, physical, doping concentration and/or doping profile characteristics. As such, the source or drain regions of a non-symmetrical device are typically not interchangeable.

The transistor 14 may be controlled using a negative drain voltage on, for example, bit line 28i, to remove holes from electrically floating body region 18 through drain 22 to write a logic low (i.e., binary state "0"). Under this circumstances, a negative voltage applied to gate 16 of the other (non-selected) memory cells in the memory array of device

5   10 may be necessary to avoid "leakage current" in other cells connected to the same bit line 28i when the negative bit line voltage is applied during the write (logic low) operation.

Other operations such as writing a logic high data state (binary "1") and reading the data may be performed using positive voltages applied to word lines 24. As such, transistors 14 of device 10 are periodically pulsed between a positive gate bias, which (1)

10   drives majority carriers (holes for N-channel transistors) away from the interface between gate insulator 32 and body region 18 of transistor 14 and (2) causes minority carriers (electrons for N-channel transistors) to flow from source region 20 and drain region 22 into a channel formed below gate 16, and a negative gate bias, which causes majority carriers (holes for N-channel transistors) to accumulate in or near the interface between gate 16

15   and body region 18 of transistor 14.

With reference to FIGURE 3A, a positive voltage applied to gate 16 provides a positive gate bias which causes (1) a channel of minority carriers 34 to form beneath gate 16 and (2) accumulation of majority carriers 30 in body region 18 in an area "opposite" the interface of gate 16 and body region 18. Here, minority carriers (i.e., electrons in an N-

20   channel transistor) may flow in the channel beneath the interface of gate oxide 32 and floating body region 18 wherein some of the minority carriers 34 are "trapped" by or in defects within the semiconductor (typically created or caused by the transition from one material type to another).

With reference to FIGURE 3B, when a negative voltage is applied to gate 16, the gate bias is negative which substantially eliminates the channel of minority carriers 34 beneath gate 16 (and gate oxide 34). However, some of minority carriers may remain "trapped" in the interface defects (illustrated generally by electrons 36).

5   Some of the trapped electrons 36 recombine with majority carriers which are attracted to gate 16 (due to the negative gate bias), and, as such, the net charge of majority carriers 30 located in floating body region 18 may decrease over time (see, for example, FIGURE 3C). This phenomenon may be characterized as charge pumping. Thus, pulsing between positive and negative gate biases (during read and write operations) may reduce

10   the net quantity of charge in memory cell 12, which, in turn, may gradually eliminate the data stored in memory cell 12.

Notably, for the efficient charge pumping phenomenon to occur, the free electron concentration at the surface (n_e) in inversion should be sufficiently large that the interface traps can capture electrons during the time the transistor is in inversion. The time constant

15   for electron capture may be characterized as:

$$\tau_e = \frac{1}{v_{th} \cdot \sigma_n \cdot n_e}$$

Accordingly, in the case $\tau_e = 3ns$ (typical pulse duration in advanced DRAM memories), the thermal velocity $v_{th} = 1 \times 10^7 cm/s$ and the capture cross section

20     $\sigma_n = 2 \times 10^{-16} cm^2$, at least $n_e \approx 2 \times 10^{17} cm^{-3}$ may be required. Analogously, in accumulation the free hole concentration at the surface (n_h) should be sufficiently large that holes can recombine with the captured electrons during the time transistor 14 is in accumulation. If $\sigma_n = \sigma_p$, $n_h \approx 2 \times 10^{17} cm^{-3}$ at least may be required (i.e., the efficient charge pumping effect

exists if the gate voltage in inversion accumulates at least $2 \times 10^{17} cm^{-3}$ electrons at the surface and the gate voltage in accumulation accumulates at least $2 \times 10^{17} cm^{-3}$ holes).

Notably, the <u>entire</u> contents of the Semiconductor Memory Device Patent Application, including, for example, the features, attributes, architectures, configurations, materials, techniques and advantages described and illustrated therein, are incorporated by reference herein.

SUMMARY OF THE INVENTION

There are many inventions described and illustrated herein. In a first principal aspect, the present invention is a semiconductor memory array comprising a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns. Each semiconductor dynamic random access memory cell includes a transistor having a source region, a drain region, a electrically floating body region disposed between and adjacent to the source region and the drain region, and a gate spaced apart from, and capacitively coupled to, the body region. Each transistor includes a first state representative of a first charge in the body region, and a second data state representative of a second charge in the body region. Further, each row of semiconductor dynamic random access memory cells includes an associated source line which is connected to only the semiconductor dynamic random access memory cells of the associated row.

In one embodiment of this aspect of the present invention, each memory cell of each row of semiconductor dynamic random access memory cells includes a separate bit line which is connected to the drain region of the associated transistor. In operation, each

memory cell of a first row is programmed to a first data state by applying a control signal, having a first amplitude, to the gate of the transistor of each memory cell of the first row and a control signal, having a second amplitude, to the drain of each memory cell of the first row. Thereafter, a predetermined memory cell of the first row may be programmed to a

5   second data state by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell, a control signal, having an fourth amplitude, to the drain of predetermined memory cell, and a control signal, having a fifth amplitude, to the source of predetermined memory cell of the row. Notably, unselected memory cell(s) of the first row is/are maintained in the first data state, while the predetermined memory cell is

10   programmed to a second data state, by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an sixth amplitude, to the drain of predetermined memory cell.

The memory cells of the first row may be read by applying a control signal, having a seventh amplitude, to the gate of the transistor of the predetermined memory cell and a

15   control signal, having an eighth amplitude, to the drain of predetermined memory cell. Notably, all of the memory cells of a second row (an unselected row) are maintained in an inhibit state while the memory cells of the first row are read. In one embodiment, the memory cells of the second row are maintained in an inhibit state (while the memory cells of the first row are read) by applying a control signal having a ninth amplitude to the gate of

20   the transistors of the memory cells of the second row.

In one embodiment, the each memory cell of a first row of semiconductor dynamic random access memory cells shares a drain region with a memory cell in a second row of semiconductor dynamic random access memory cells, wherein the first and second rows of

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memory cells are adjacent rows. In another embodiment, each gate of each memory cell of a first row of semiconductor dynamic random access memory cells is connected to a first gate line. In yet another embodiment, the gate of each memory cell of the first row of semiconductor dynamic random access memory cells is connected to the first gate line.

5   In another principal aspect, the present invention is a semiconductor memory array comprising a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns. Again, each semiconductor dynamic random access memory cell includes a transistor having a source region, a drain region, a electrically floating body region disposed between and adjacent to the source region and the drain

10   region, and a gate spaced apart from, and capacitively coupled to, the body region. Each transistor includes a first state representative of a first charge in the body region, and a second data state representative of a second charge in the body region.

In this aspect, the each row of semiconductor dynamic random access memory cells includes (1) an associated source line which is connected to only the semiconductor

15   dynamic random access memory cells in the associated row and (2) a different gate line for each semiconductor dynamic random access memory cells in the associated row.

In one embodiment of this aspect of the present invention, each memory cell of each row of semiconductor dynamic random access memory cells includes a separate bit line which is connected to the drain region of the associated transistor. In operation, each

20   memory cell of a first row is programmed to a first data state by applying a control signal, having a first amplitude, to the gate of the transistor of each memory cell of the first row and a control signal, having a second amplitude, to the drain of each memory cell of the first row. Thereafter, a predetermined memory cell of the first row may be programmed to a

second data state by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell, a control signal, having a fourth amplitude, to the drain of predetermined memory cell, and a control signal, having a fifth amplitude, to the source of predetermined memory cell of the row. Notably, unselected memory cell(s) of

5   the first row is/are maintained in the first data state, while the predetermined memory cell is programmed to a second data state, by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having a sixth amplitude, to the drain of predetermined memory cell.

The memory cells of the first row may be read by applying a control signal, having a

10   seventh amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an eighth amplitude, to the drain of predetermined memory cell. Notably, all of the memory cells of a second row (an unselected row) are maintained in an inhibit state while the memory cells of the first row are read. In one embodiment, the memory cells of the second row are maintained in an inhibit state (while the memory cells

15   of the first row are read) by applying a control signal having a ninth amplitude to the gate of the transistors of the memory cells of the second row.

In one embodiment, the each memory cell of a first row of semiconductor dynamic random access memory cells shares a drain region with a memory cell in a second row of semiconductor dynamic random access memory cells, wherein the first and second rows of

20   memory cells are adjacent rows. In another embodiment, each gate of each memory cell of a first row of semiconductor dynamic random access memory cells is connected to a first gate line.

Again, there are many inventions described and illustrated herein. This Summary of the Invention is not exhaustive of the scope of the present invention. Moreover, this Summary is not intended to be limiting of the invention and should not be interpreted in that manner. While certain embodiments, features, attributes and advantages of the inventions

5   have been described in this Summary, it should be understood that many others, as well as different and/or similar embodiments, features, attributes and/or advantages of the present inventions, which are apparent from the description, illustrations and claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

In the course of the detailed description to follow, reference will be made to the

10   attached drawings. These drawings show different aspects of the present invention and, where appropriate, reference numerals illustrating like structures, components, materials and/or elements in different figures are labeled similarly. It is understood that various combinations of the structures, components, materials and/or elements, other than those specifically shown, are contemplated and are within the scope of the present invention.

15   FIGURE 1A is a schematic representation of a semiconductor DRAM array as illustrated (and described) in the Semiconductor Memory Device Patent Application;

FIGURE 1B illustrates a memory cell according to the Semiconductor Memory Device Patent Application;

FIGURES 2A and 2B are exemplary schematic illustrations of the charge

20   relationship, for a particular memory state, of the floating body, source and drain regions of a memory cell according to the Semiconductor Memory Device Patent Application;

FIGURES 3A-3C are exemplary schematic and general illustrations of the charge relationship and charge pumping phenomenon caused by pulsing between positive and negative gate biases (during read and write operations) of the memory cell of FIGURE 1B;

FIGURE 4 is a tabulation of exemplary voltage pulse levels that may be employed in 5 a method of a first embodiment of the present invention;

FIGURE 5 is a tabulation of exemplary voltage pulse levels that may be employed in a method of a second embodiment of the present invention;

FIGURE 6 is a tabulation of exemplary voltage pulse levels that may be employed in a method of a third embodiment of the present invention;

10 FIGURE 7 is a tabulation of exemplary voltage pulse levels that may be employed in a method of an embodiment of the present invention;

FIGURE 8 illustrates an exemplary word (gate) line voltage waveform to be used in a method of a fourth embodiment of the present invention;

FIGURE 9 illustrates an exemplary word (gate) line voltage waveform to be used in 15 a method of a fifth embodiment of the present invention;

FIGURE 10 illustrates a timing relationship between exemplary word (gate) line and the bit line voltage waveforms of the fourth embodiment of the present invention;

FIGURE 11 is a schematic representation of semiconductor DRAM memory device according to an aspect of present invention;

20 FIGURE 12 is a schematic representation of column sense and refresh circuitry that may be employed in the semiconductor DRAM memory device of FIGURE 11;

FIGURES 13A, 13B, 14A and 14B illustrate a memory array including a plurality of memory cells having a separate source line array that define a particular row of memory

cells, and exemplary writing and/or programming techniques (including exemplary programming voltage values), according to another aspect of the present invention;

FIGURES 15A and 15B illustrate read operations, including exemplary read operation voltage values, according to an embodiment of the present invention, for the

5   memory array of FIGURES 13A, 13B, 14A and 14B;

FIGURE 16 illustrates an exemplary layout of the memory array of FIGURES 13A, 13B, 14A and 14B;

FIGURES 17 and 18 illustrate another memory array architecture including a plurality of memory cells having a common source line array, and writing and/or

10   programming techniques (including exemplary programming voltage values), according to another aspect of the present invention;

FIGURE 19 illustrates exemplary read operation voltage values, according to an embodiment of the present invention, for the memory array of FIGURES 17 and 18;

FIGURE 20 illustrates an exemplary layout of the memory array of FIGURES 17 and

15   18;

FIGURE 21 illustrates a memory array including a plurality of memory cells having a separate source line array (that define a particular row of memory cells) and gates lines that are parallel to associated bit lines, and exemplary writing and/or programming techniques (including exemplary programming voltage values), according to another aspect of the

20   present invention;

FIGURE 22 illustrates exemplary read operation voltage values, according to an embodiment of the present invention, for the memory array of FIGURE 21;

FIGURE 23 illustrates an exemplary layout of the memory array of FIGURES 21 and 22;

FIGURES 24 and 25 illustrate another memory array architecture including a plurality of memory cells having a common source line array, and writing and/or programming techniques (including exemplary programming voltage values), according to another aspect of the present invention;

FIGURE 26 illustrates exemplary read operation voltage values, according to an embodiment of the present invention, for a memory array of FIGURES 25 and 26;

FIGURE 27 illustrates an exemplary layout of the memory array of FIGURES 24 and 25;

FIGURE 28 illustrates an exemplary configuration of a dual-port or a multi-port memory cell, according to another aspect of the present invention; and

FIGURE 29 illustrates an exemplary layout of the dual-port or a multi-port memory cell of FIGURE 28.

DETAILED DESCRIPTION

There are many inventions described and illustrated herein. In a first aspect, the present invention is directed to a memory device and technique of reading data from and writing data into memory cells of the memory device. In this regard, in one embodiment of this aspect of the invention, the memory device and technique for operating that device that minimizes, reduces and/or eliminates the debilitating affects of the charge pumping

phenomenon. This embodiment of the present invention employs control signals that minimize, reduce and/or eliminate transitions of the amplitudes and/or polarities.

With reference to FIGURES 1 and 4, in one embodiment, transistor 14 (a 0.25 micron N-channel MOSFET DRAM cell) may be operated using the exemplary voltage
5   values. In this regard, a write logic low (binary data state "0") operation, in one exemplary embodiment, may be written by applying a word line (i.e., gate bias) voltage of 2.9V, and the bit line (here, a drain bias) voltage of 2.3V. In this operation, the source line voltage is maintained at 0V. Under these conditions, the junction between body region 18 and source region 20 is forward biased, and excess holes are removed from body region 18 into
10   source region 20.

To perform a write logic high (binary data state "1") in transistor 14, a voltage of 0.6V is applied to gate 16 (i.e., the gate bias is held at 0.6V) and a voltage of 2.3V is applied to drain 22. In response, an electric current between source region 20 and drain region 22 providing impact ionization in body region 18, which in turn generates excess majority
15   carriers (holes) in body region 18. Note that the gate voltage of unselected cells (holding voltage) is kept at 0V. It is found that these exemplary voltages avoid strong accumulation of holes at the interface of gate oxide 32 and floating body region 18 wherein minority carriers 34 have a tendency to be "trapped" by or in defects within the semiconductor. In this way, disturbance of data caused by charge pumping is suppressed, reduced,
20   minimized and/or eliminated.

In a second embodiment, with reference to FIGURES 1 and 5, transistor 14 (a 0.25 micron N-channel MOSFET DRAM cell) may be operated using the exemplary voltage values indicated. In this regard, to write a logic high (binary data state "1"), a strong

accumulation of majority carriers at the interface of gate oxide 32 and floating body region 18 is required. In one exemplary embodiment, a voltage of -1.7V is applied to gate 16 and a voltage of 1.7V is applied to drain region 22 to provide the strong accumulation of majority carrier at the interface of gate oxide 32 and floating body region 18. These control

5   signals cause deformation of the valence and conduction bands at the interface between body region 18 and source region 20. As a result, minority carriers (here, electrons) are injected into the conduction band by means of a tunnel effect (an effect known as gate induced drain leakage (GIDL)), which in turn causes the generation of majority carriers (here, holes) in body region 18. This operating technique has an advantage in that hole

10   generation occurs in a non-conducting state of transistor 14. In this way, majority carrier generation may be achieved at a relatively lower power consumption.

To perform a read data operation, in one embodiment, an inversion channel is created at the interface of gate oxide 32 and floating body region 18. This may be achieved by applying a voltage of 0V to gate 16 and drain region 22 (i.e., a gate bias of 0V)

15   and a voltage of -0.5V to source region 20.

In a third embodiment, with reference to FIGURES 1 and 6, transistor 14 (a 0.13 micron technology DRAM cell) may be programmed and/or operated using the exemplary voltages indicated. The voltages set forth in FIGURE 6 represent "ideal" conditions, in which the application of the voltage pulses does not disturb the data stored within the cell.

20   However, the cells are arranged in matrices in which some cells are accessed when others remain un-accessed, and column and row decoding are therefore necessary to enable the matrices to function. This results in voltage levels differing from the levels being applied during write, read and hold operations (in practice, all of the cells that share either the same

column or row with the addressed memory cell), as a consequence of which disturbance of the data stored within those cells may occur.

An example of this is shown in FIGURES 1 and 7, in which data state "0" is being written to memory cell 12 at the intersection of the selected word line and bit line. Since all 5 cells in the same column of FIGURE 1 share the same gate voltage and all cells in the same row as FIGURE 7 share the same drain voltage, voltages different from the "ideal" holding voltages are applied to those memory cells, as a result of which charge may leak from the floating body regions of those cells.

Similar arrangements occur when writing logic high (i.e., data state "1") or reading 10 the data from memory cells 12. It is found (experimentally) that a worst case is represented by writing logic low (i.e., data state "0"), and memory cells 14 may sustain a few hundred cycles of word line switching, and over 10,000 cycles of bit line switching. It can therefore be seen that fluctuations in the gate voltage may impose limitations on the architecture of the circuit, and in particular, if it is assumed that only 100 cycles of word line pulsing are 15 permissible, this small number of cycles could either necessitate partitioning the rows to smaller length (e.g., 64) or refreshing all cells along the word line as frequently as on a prior art DRAM involving transistors and capacitors.

Both of these arrangements are extremely inefficient since they could significantly increase the number of word line drivers or sense amplifiers required to operate the circuit. 20 Furthermore, because each data cell is smaller (4F2) than a conventional DRAM cell (8F2), the circuit layout may be either impossible or extremely expensive to achieve.

With reference to FIGURES 8, 11 and 12, in one embodiment, the number of word line drivers and/or sense amplifiers are reduced and/or minimized. In this regard, a column

decoder is disposed or arranged between the bit lines and the sense amplifiers to reduce and/or minimize the number of sense amplifiers and, in conjunction, while only one cell in a block (typically 8 or 16) is read. The memory cell on a column defined by an internal counter (for example, among 8 or 16) and on a row defined by user addresses is read and

5   thereafter, refreshed. That cell then is available for user access (via read or write operation) at the same row and column defined by the user addresses.

From a signaling perspective, with reference to FIGURE 8, the variations or swings of the amplitude, as well as the polarity, of the gate voltages are reduced and/or minimized in number and rising/falling edges. Notably, a read or write operation of a predetermined

10   memory cell may occur prior to the refresh operation. (See, for example, FIGURE 9).

With reference to FIGURES 11 and 12, the semiconductor DRAM memory device of this aspect of the present invention includes a plurality of matrices 40a-n, each including a plurality of memory cells 12 (comprised of transistors 14). The memory cells 12 are arranged in arrays having rows and columns, which may be addressed by content address

15   memory (CAM) 42 and column refresh counter 44. The column address output from column refresh counter 44 is applied to column address multiplexer 46. The column address multiplexer 46 receives the refresh address and the user address and provides one of the addresses to a column multiplexer 48 to select one of, for example, eight or sixteen bit lines (columns) 28a.

20   In order to enable memory cells 12 to be refreshed during, for example, idle periods (i.e., when there is no user access), memory cell 12 at the intersection of a given or selected row and a given or selected column is addressed by applying a signal on row address bus 50 to all of the interconnected gates of the row and a signal on column

address bus 52 to all of the interconnected drains of the column. The row to be refreshed is identified by row refresh counter 54, which is gated, via row address multiplexer 56, with a row address from user address bus 58.

The column refresh counter 44 supplies a column address of a column to be refreshed. As mentioned above, the column address is gated, via column address multiplexer 46, with a column address from user address bus 58. As a result, the data state of memory cell 12 at the intersection of the selected row and column is determined and re-written to memory cell 12. The column refresh counter 44 may then increment in response to the same row being chosen, as a result of which the columns are sequentially addressed for each row, regardless of the order in which the rows are addressed. This provides the advantage of minimizing the risk that a memory cell 12 fails to be refreshed within the appropriate period. Depending on the phase during access, the column addresses are received from row refresh counter 44 or from user address bus 58, and when, for example, the device (or portion thereof) is idle, the row addresses are provided by row refresh counter 54.

Notably, the refresh technique and circuitry of FIGURE 11 may be used with several arrays in parallel, as a result of which the number of sense amplifier 60 may be reduced and/or minimized (as is the area required for such circuitry on the die).

With reference to FIGURE 12, when a column is selected, the signal on WLDPW line 62 provides a power supply voltage to word line drivers 62a-x, according to the phase in the cycle waveform. The column multiplexer 48 addresses the column (and therefore the selected memory cell) to be refreshed, and the data in the selected memory cell is read by sense amplifier 60, the result being output (i.e., DATA signal) on signal line 66.

According to the signal logic levels on line 62 (after conversion by voltage converter 68) and line 66, the write conditions applied to the word line are as follows: During write "1" condition, if the DATA signal is "1", XNOR logic gate 68 outputs, on signal line 68, a logic high (i.e., binary "1") which is amplified by write amplifier 72 and then applied to the

5 selected memory cell in order to restore the data state in the selected memory cell. If the DATA signal is "0", a logic low (i.e., "0") is applied to the bit line, which represents a holding condition. While writing data state "0", on the other hand, if the DATA signal is "0", the XNOR logic gate 68 outputs a logic high (i.e., binary "1"), which is amplified by write amplifier 72 and then applied to the memory cell to restore its data. If the DATA signal is

10 "1", a "0" is applied to the bit line, which again represents a holding condition.

In certain embodiments, it may be advantageous to further reduce, minimize and/or eliminate any issues of disturbance (for example, issues of stored charge loss or gain within memory cells) of the data states of memory cells having common gate lines, drain lines and/or source lines with those memory cells that are being accessed (i.e., being read from

15 or written to during, for example, a normal or refresh operation). In one embodiment, a two-step write operation may be employed to program memory cell 12 with little to no disturbance to adjacent and/or neighboring cells (i.e., cells that share source lines, drain lines and/or gate lines). In this regard, an entire row of memory cells may first be written to the same logic state and thereafter, individual bits are written to the opposite state in

20 accordance with a desired data state (i.e., the individual bits are written to another state to reflect a desired data state).

It is intended that such two step write technique may be employed using many different memory cells and many different memory array architectures, whether now known

or later developed; and all such memory cells and different memory array architectures fall within the present invention. For example, the write technique may be implemented where memory cells 12a-d of each row 80a-f of transistors have a dedicated source line to minimize, reduce and/or eliminate disturbance on adjacent rows (for example, row 80b

5   versus row 80c).

With reference to FIGURES 13A and 13B, in one embodiment, a given row 80a-f may be written to by applying a clear operation followed by a selective write operation. In this regard, a plurality of memory cells 100, having gates that are connected to a common gate line, are arranged to form row 80a. Exemplary voltages that implement a clear

10   operation for row 80a and maintain the remaining portion of the array (i.e., rows 80b-f) in a fixed state (i.e., unchanged in response to the clear operation) are indicated in FIGURES 13A and 13B. In response, the same logic state (for example, logic high or binary "1") is stored in memory cells 12a-d of row 80a. In this way, the state of memory cells 12a-d are "cleared".

15   Thereafter, individual transistors of memory cells 12a-d of row 80a are written to a particular, desired and/or predetermined logic state (see, for example, FIGURES 14A and 14B) in order to store the particular, desired and/or predetermined logic state in memory cells 12a-d. In particular, with reference to FIGURE 14A, as described above, memory cells 12a-d are set to logic high (binary "1") by the clear operation, and then memory cells

20   12b and 12d are written to logic low (binary "0"). Notably, the logic state of memory cells 12a and 12c remains logic high during the write operation (via applying an inhibit voltage to the associated bit lines 28a and 28c (FIGURE 14A). With reference to FIGURE 14B, memory cells 12a-d are cleared to logic high (binary "1") and then memory cells 12a and

12d are written to logic low (binary "0"). Memory cells 12b and 12c remain logic high via a write inhibit voltage applied to associated bit lines 28b and 28c.

With reference to FIGURES 15A and 15B, the data may be read from memory cells 12a-d of row 80b by applying the exemplary voltages indicated. An exemplary holding

5   voltage for the remaining portion of the array (including the memory cells of row 80b-f) is also indicated. The holding voltage/signal maintains the unselected portion of the array in a fixed state (i.e., unchanged in response to the read operation). Notably, the exemplary read and holding voltages of FIGURES 15A and 15B may avoid, reduce and/or minimize charge pumping disturb.

10   Thus, in this embodiment, the first step of the write operation clears the memory cells having a common source line and the second step writes or stores new data or the previous data (in the event that the data did not change). Array architectures employing this write operation technique may have an advantage that the unselected memory cells of the array are not "disturbed" (or experience little and/or negligible disturbance) because

15   "high" voltages are applied in the row direction (i.e., on source lines 26) but not in the column direction (i.e., on the drain or bit lines 28). This write technique may be performed as a page mode write where the page is first "cleared" and then individual bytes (or bits) in a page are written to a new state.

Notably, the memory architecture, write and/or programming techniques, and read

20   techniques of FIGURES 13A, 13B, 14A, 14B, 15A and 15B may be implemented in conjunction with the embodiments of the device of FIGURES 11 and 12. For the sake of brevity, those discussions will not be repeated.

FIGURES 17-20 illustrate another memory array architecture in which a plurality of memory cells "share" a source line and employ the two-step write technique that may eliminate, minimize and/or reduce disturbance to memory cells when reading from and/or writing to adjacent memory cells. In this regard, with reference to FIGURES 17 and 18, in one embodiment, a given row may be written to by applying suitable voltages to implement a clear operation (FIGURE 17) followed by a selective write operation (FIGURE 18). In conjunction with applying suitable voltages to implement the clear operation, a write inhibit signal is applied to the gates of memory cells that share a source line 26 (for example, a write inhibit signal may be applied to the gates of the memory cell of row 80b). Notably, any disturbance on unselected, adjacent row 80b (with respect to row 80a), may avoid, reduce and/or minimize by biasing word line 24b to an intermediate value that balances write logic low (i.e., write "0") and write logic high (i.e., write "1") operation.

In particular, exemplary voltages that implement a clear operation for row 80a and maintain the neighboring memory cells (for example, memory cells of row 80b) remaining portion of the array in a fixed state (i.e., unchanged in response to the clear operation) are indicated in FIGURE 17. The memory cells 12a-d of row 80a are written to a particular, desired and/or predetermined logic state (see, for example, FIGURE 18 (write "0") in memory cell 12a and memory cell 12d and (write "1") in memory cell 12b and memory cell 12c) in order to store a particular, desired and/or predetermined logic state of memory cell 12.

With reference to FIGURE 19, the data may be read from memory cells 12a-d of row 80a by applying the exemplary voltages indicated. Notably, an exemplary holding voltage for the remaining portion of the array (including the neighboring memory cells of row 80b as

well as the memory cells of rows 80c-f) is also indicated. The holding voltage/signal maintains the unselected portion of the array in a fixed state (i.e., unchanged in response to the read or write operation).

The memory architecture, write and/or programming techniques, and read techniques of FIGURES 17-20 may be implemented in conjunction with the embodiments of the device of FIGURES 11 and 12. For the sake of brevity, those discussions will not be repeated.

Another memory array architecture that may employ a one-step write technique that eliminates, minimizes and/or reduces disturbance to memory cells when reading from and/or writing to adjacent memory cells is illustrated in FIGURES 21-23. In this architecture, source lines 26 are separated for each row 80a-e. In addition, word lines 24a-d are arranged parallel to associated bit lines 28a-d, respectively.

With reference to FIGURE 21, in one embodiment, a given row may be written to by applying suitable voltages to directly implement a write operation (see, memory cells 12a-d of row 80a). In conjunction with applying suitable voltages to implement the write operation, a write inhibit signal is applied to source lines 26b-e of rows 80b-e, respectively. Exemplary voltages that implement the write operation (for memory cells 12a-d) and the inhibit state (for the memory cells of rows 80b-e) are indicated in FIGURE 21. The memory cells 12a and 12d of row 80a are maintained and/or written to a particular, desired and/or predetermined logic state (here, write "1") and memory cells 12b and 12c are written to a different desired and/or predetermined logic state (here, write "0").

With reference to FIGURE 22, the data may be read from memory cell 12a of row 80a by applying the exemplary voltages indicated. Notably, an exemplary read inhibit

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voltage for the remaining portion of the array (including the other memory cells of row 80a and the memory cells of rows 80d-e) is also indicated. The read inhibit voltage/signal maintains the unselected portion of the array in a fixed state (i.e., unchanged in response to the read operation).

5   The memory architecture, write and/or programming techniques, and read techniques of FIGURES 21-23 may be implemented in conjunction with the embodiments of the device of FIGURES 11 and 12. For the sake of brevity, those discussions will not be repeated.

Another memory array architecture that may employ the two-step write technique
10   that eliminates, minimizes and/or reduces disturbance to memory cells when reading from and/or writing to adjacent memory cells is illustrated in FIGURES 24-27. In this architecture, the source lines are shared but bit lines are separated so each memory cell on either side of a source line, for example memory cells 12, has a dedicated bit line. The gates of transistors 12a and 12e may be connected together at the array boundary.

15   Notably, memory cells 12a and 12e are located on separate rows with the gates of each transistor 12a and 12e connected at, for example, the array boundary. In this embodiment, there is a separate bit line (here, drain lines 28a and 28e) for each memory cell 12a and 12e so that each transistor 12a and 12e may be read separately.

With reference to FIGURES 24-27, in one embodiment, a given pair of rows may be
20   written to by applying suitable voltage to implement a clear operation (FIGURE 24) followed by a selective write operation (FIGURE 25). The pair of rows (for example, rows 80a and 80b) corresponding to memory cells 12a and 12e, on either side of a common source line, are written and read (FIGURE 26) simultaneously.

Notably, the memory architecture, write and/or programming techniques, and read techniques of FIGURES 24-27 may be implemented in conjunction with the embodiments of the device of FIGURES 11 and 12. For the sake of brevity, those discussions will not be repeated.

5   There are many inventions described and illustrated herein. While certain embodiments, features, materials, configurations, attributes and advantages of the inventions have been described and illustrated, it should be understood that many other, as well as different and/or similar embodiments, features, materials, configurations, attributes, structures and advantages of the present inventions that are apparent from the description,

10   illustration and claims. As such, the embodiments, features, materials, configurations, attributes, structures and advantages of the inventions described and illustrated herein are not exhaustive and it should be understood that such other, similar, as well as different, embodiments, features, materials, configurations, attributes, structures and advantages of the present inventions are within the scope of the present invention.

15   For example, as mentioned above, the illustrated voltage levels to implement the write and read operations are exemplary. The indicated voltage levels may be relative or absolute. That is, for example, a logic low may be written into transistor 102a (see, for example, FIGURE 13A) using the voltages indicated therein. Alternatively, the voltages indicated may be relative in that each voltage level, for example, may be increased or

20   decreased by a given voltage amount (for example, each voltage may be increased by 0.25 volts).

Moreover, while a significant portion of this description includes details (for example, clear, write, read and inhibit voltages) directed to N-channel transistors, the inventions (and

embodiments thereof) described herein are entirely applicable to P-channel transistors. In such embodiments, majority carriers 30 in body region 18 are electrons and minority carriers 34 are holes. Indeed, the memory arrays of matrices 40a-n may be comprised of N-channel, P-channel and/or both types of transistors. Moreover, the circuitry that is

5 peripheral to the memory array (for example, row and column address decoders, not illustrated herein, as well as comparators) may include P-channel and/or N-channel type transistors, including transistors like transistor 14.

Notably, where P-channel type transistors are employed as memory cells 12 in the memory array(s) of matrices 40a-n, suitable clear, write, read and inhibit voltages are well

10 known to those skilled in the art in light of this disclosure. Accordingly, for sake of brevity, these discussions will not be repeated.

Further, memory cell(s) 12 (as well as memory array and matrices 40a-n) may also employ the structure, features, attributes, architectures, configurations, materials, techniques and advantages described and illustrated in non-provisional patent application

15 entitled "Semiconductor Device", which was filed on February 18, 2004, by Fazan and Okhonin, and assigned Serial No. 10/487,157 (hereinafter "Semiconductor Device Patent Application"). The entire contents of the Semiconductor Device Patent Application, including, for example, the inventions, features, attributes, architectures, configurations, materials, techniques and advantages described and illustrated therein, are hereby

20 incorporated by reference herein.

Furthermore, the memory transistors and/or cells, and method of operating such transistors and/or cells, of the present invention may be implemented in many different configurations. For example, the floating body regions of two or more transistors may be

shared to realize a dual-port or a multi-port memory cell. In this regard, with reference to FIGURE 28, a dual port memory cell 12a may include transistors 14a and 14b. A dual port memory array may include a plurality of dual port memory cells 12 arranged, for example, in a matrix of rows and columns. The data state defined by the amount of carriers in the

5   common electrically floating body region 18 is common to the two transistors 14a and 14b.

The read and write access operations may be performed independently for transistors 14a or 14b, using the respective independent word lines 24, source line 26 and bit lines 28. In the illustrative example, source line 26 is common to the transistors 14a and 14b of memory cell 12a. Notably, the source regions of transistors 14a and 14b may be

10   connected to separate source lines.

With reference to FIGURE 29, in an exemplary layout, dual port memory cell 12a includes a P+ floating body node 18 that "connects" a P- floating body region under gate 24m of transistor 14a with a P- floating body region under gate 24n of transistor 14b. The gates 24m and 24n are connected to word lines 24m and 24n, respectively. The source

15   regions 20a and 20b are connected to respective source lines. The drain regions 22a and 22b are connected to drain lines. Notably, as mentioned above, although this description includes details directed to N-channel transistors, the inventions (and embodiments hereof) are entirely applicable to P-channel transistors. In such embodiments, majority carriers in body region 18 are electrons, and minority carriers are holes.

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